AMENDMENTS

In the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

1-54. (Cancelled)

55. (Previously Presented) A semiconductor device, comprising:

a field effect transistor formed on a semi-insulating substrate and comprising a gate electrode, a source electrode and a drain electrode;

a bonding pad formed on the semi-insulating substrate and connected to the gate electrode, the source electrode or the drain electrode; and

a protecting element for the transistor formed on the semi-insulating substrate and connected between the bonding pad and a terminal of one of the electrodes that is not connected to the bonding pad, the protecting element comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region disposed between the first and second high concentration impurity regions and being configured to permit current flow between the first and second high concentration impurity regions upon application between the bonding pad and the terminal of an electrostatic energy that is larger than a predetermined amount,

wherein the first high concentration impurity region is closer to the bonding pad than the second high concentration impurity region, electrically disconnected from the bonding pad except during the application of the electrostatic energy, physically separated from the bonding pad so as to form a Schottky junction between the bonding pad and a portion of the semi-insulating substrate in which the first high concentration impurity region is not formed, and configured to be electrically connected to the bonding pad through the Schottky junction so as to permit the current flow upon the application of the electrostatic energy.

56. (Previously Presented) The semiconductor device of claim 55, wherein the first high concentration impurity region is disposed along at least one side of the bonding pad.

57. (Previously Presented) The semiconductor device of claim 55, further comprising a peripheral high concentration impurity region disposed at a peripheral area of the bonding pad, wherein the first high concentration impurity region is part of the peripheral high concentration impurity region.

58. (Previously Presented) The semiconductor device of claim 55, wherein the protecting element is placed in a path extending from the terminal to an operation region of the field effect transistor.

59. (Previously Presented) The semiconductor device of claim 55, further comprising:

an additional bonding pad provided as the terminal; and

a resistor connected to the additional bonding pad and comprising a resistor high concentration impurity region,

wherein the second high concentration impurity region is at least part of the resistor high concentration impurity region.

60-62. (Cancelled)

63. (Previously Presented) The semiconductor device of claim 55, further comprising an additional protecting element for the transistor connected between the bonding pad and another terminal of the electrodes that is not connected to the bonding pad, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application between the bonding pad and the another terminal of an electrostatic energy that is larger than a predetermined amount, wherein the protecting element is disposed along a side of the bonding pad and the additional protecting element is disposed along another side of the bonding pad.

64. (Previously Presented) The semiconductor device of claim 55, further comprising:

an additional field effect transistor comprising a gate electrode, a source electrode and a drain electrode; and

an additional protecting element connected between the bonding pad and a terminal of one of the electrodes of the additional field effect transistor, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application of an electrostatic energy that is larger than a predetermined amount between the bonding pad and the terminal of the additional filed effect transistor,

wherein the protecting element is disposed along a side of the bonding pad and the additional protecting element is disposed along another side of the bonding pad.

65. (Previously Presented) The semiconductor device of claim 55, further comprising:

an additional bonding pad provided as another terminal of the electrodes; and

an additional protecting element for the transistor connected between the terminal and the additional bonding pad, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application between the terminal and the additional bonding pad of an electrostatic energy that is larger than a predetermined amount,

wherein at least part of the first additional high concentration impurity region is disposed under the additional bonding pad or in close proximity to the additional bonding pad to permit the current flow upon the application of the electrostatic energy.

66. (Previously Presented) The semiconductor device of claim 65, wherein the protecting element and the additional protecting element are placed in a path extending from the terminal to an operation region of the field effect transistor.

67-83. (Cancelled)

84. (Currently Amended) A semiconductor switching device, comprising:

a first field effect transistor comprising a gate electrode, a source electrode and a drain electrode;

a second field effect transistor comprising a gate electrode, a source electrode and a drain electrode;

a common input terminal connected to the source or drain electrode of the first transistor and to the source or drain electrode of the second transistor;

a first control terminal connected to the gate electrode of the first or second transistor;

a second control terminal connected to the gate electrode of the first or second transistor that is not connected to the first control terminal;

a first resistor connecting the first control terminal and a corresponding gate electrode and comprising a first resistor high concentration impurity region;

a second resistor connecting the second control terminal and a corresponding gate electrode and comprising a second resistor high concentration impurity region;

a first output terminal connected to the source or drain electrode of the first transistor that is not connected to the common input terminal;

a second output terminal connected to the source or drain electrode of the second transistor that is not connected to the common input terminal; and

a protecting element connected between the common input terminal and the first control terminal, the protecting element comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region disposed between the first and second high concentration impurity regions and being configured to permit current flow between the first and second high concentration impurity regions upon application between the common

input terminal and the first control terminal of an electrostatic energy that is larger than a predetermined amount, the first high concentration impurity region being at least part of the first resistor high concentration impurity region, the first and second high concentration impurity regions being electrically disconnected from each other except during the application of the electrostatic energy, and no electrical wiring existing between the first and second high concentration impurity regions,

wherein the common input terminal comprises a bonding pad,

a peripheral high concentration impurity region is disposed at a peripheral area of the bonding pad, and

the second high concentration impurity region is part of the peripheral high concentration impurity region.

85. (Previously Presented) The semiconductor switching device of claim 84, further comprising an additional protecting element connected between the first control terminal and the first output terminal or between the second control terminal and the second output terminal, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application between the corresponding terminals of an electrostatic energy that is larger than a predetermined amount, the first additional high concentration impurity region being at least part of the first resistor high concentration impurity region or the second resistor high concentration impurity region.

86. (Cancelled)

87. (Previously Presented) The semiconductor switching device of claim 84, further comprising an additional protecting element connected between the common input terminal and the second control terminal, the additional protecting element comprising a first additional high concentration impurity region, a second additional high concentration impurity region and an

additional insulating region disposed between the first and second additional high concentration impurity regions and the additional protecting element being configured to permit current flow between the first and second additional high concentration impurity regions upon application between the corresponding terminals of an electrostatic energy that is larger than a predetermined amount, the first additional high concentration impurity region being at least part of the second resistor high concentration impurity region, wherein the protecting element is disposed along a side of the common input terminal and the additional protecting element is disposed along another side of the common input terminal.

88. (Cancelled)

89. (Currently Amended) The semiconductor switching device of claim [[88]] 84, wherein the second high concentration impurity region is disposed along at least one side of the bonding pad.

90. (Previously Presented) The semiconductor switching device of claim 84, wherein the common input terminal comprises a bonding pad, and at least part of the second high concentration impurity region is placed in close proximity to the bonding pad to permit the current flow upon the application of the electrostatic energy.

91. (Previously Presented) The semiconductor switching device of claim 90, wherein the second high concentration impurity region is disposed along at least one side of the bonding pad.

92. (Cancelled)

93. (Previously Presented) The semiconductor switching device of claim 90, further comprising a peripheral high concentration impurity region disposed at a peripheral area of the bonding pad, wherein the second high concentration impurity region is part of the peripheral high concentration impurity region.

94-97. (Cancelled)